REMARKS

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakaedani et al. (US 6,064,360) in view of Moon (US 5,793,346). Applicant respectfully traverses the rejection for at least the following reasons.

The Office Action asserts that Sakaedani et al. teaches, in FIGs. 1 and 4, a discharge circuit 35 to discharge first and second voltage supply lines Vgh and Vgl, thereby discharging voltages on the gate lines 32. In addition, the Office Action admits that Sakaedani et al. "does not specifically teach the discharge circuit for sensing a power-off condition of the power supply line to short circuit when the power-off condition is sensed. Accordingly, the Office Action relies upon Moon for allegedly teaching "a discharge circuit (40) for sensing (41) a power-off condition of the power supply lines to short circuit (M1) the voltage supply line when the power-off condition is sensed (from col. 3, line 50 to col. 4, line 11)." Thus, the Office Action concludes that it would have been obvious to combine the teachings of Moon with the system of Sakaedani et al. to reduce a residual image upon power-off. Applicant respectfully disagrees.

In contrast to Applicant's claimed invention and contrary to allegations of the Office Action, the afterimage circuit 35 of Sakaedani et al., as shown in FIG. 3, raises the potential of unselected gate lines 31 by about +2V to forcibly discharge the active switching element 31 by providing stored charge in the capacitor C1 to the gate line driver circuit 33 *when the supply of power to the liquid crystal display is stopped.* Thus, the afterimage circuit 35 of Sakaedani et al. fails to short-circuit the first and second gate voltage lines "when the power-off condition is sensed," as recited by independent claim 1.

In further contrast to Applicant's claimed invention and further contrary to allegations of the Office Action, Moon fails to remedy the deficiencies of Sakaedani et al. For example, Moon teaches, in FIG. 4, the use of a screen clearing circuit 40 including a power shut-off detecting circuit 41 that detects whether external power VDD is being supplied. Accordingly, Moon teaches (col. 3, lines 52) "the GND voltage level is applied to the gates of the TFTs, thereby turning off the LCD display by providing a path to discharge the liquid crystal capacitor Clc and the support capacitor Cst electrically coupled thereto." Thus, Applicant respectfully asserts that Moon is completely silent with respect to short-circuiting first and second gate voltage supply lines that supply first and second gate voltages to gate driver circuitry, as required by independent claim 1, and hence dependent claims 2-7.

For at least the above reasons, Applicant respectfully submits that claims 1-7 are neither taught nor suggested by any of the applied prior art references, whether taken alone or in combination. Applicant respectfully asserts that the rejections under 35 U.S.C. § 103(a) should be withdrawn because the above-discussed novel combinations of features are neither taught nor suggested by any of the applies references, whether taken alone or in combination.

CONCLUSION

In view of the foregoing, Applicant respectfully requests entry of the remarks, reconsideration and the timely allowance of all pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such as an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

By: _____
David B. Hardy
Reg. No. 47,362

Date: August 12, 2004

CUSTOMER NO. 009629
MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
(202) 739-3000